Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	9101	embedded near6 processor	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/18 09:21
L2	1354	"built in self test"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/18 09:26
L3	227	"pseudo-random pattern generator"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/18 09:23
L4	1908	lfsr	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/18 09:24
L5	2050	l3 or l4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/18 09:24
L6	0	l1 with l5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/18 09:24
L7	5	l1 same l5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/18 09:25
L8	147	l1 and l5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/18 09:24
L9	143	l2 same processor	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/18 09:26
L10	209	l2 same controller	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/18 09:26

L11	259	l9 or l10	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/18 09:31
L12	8	l11 same l5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/18 09:27

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	129	"scan path testing"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/18 09:00
L2	3509	"embedded processor"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/18 09:00
L3	71517	"non volatile memory"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/18 09:01
L4	227	"pseudo-random pattern generator"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/18 09:04
L5	0	l1 with l2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/18 09:02
L6	0	l1 same l2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/18 09:02
L7	1	l1 and l2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/18 09:03
L8	0	l2 same l4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/18 09:03
L9	0	l2 and l4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/18 09:03

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	89	(714/728).CCLS.	USPAT	OR	OFF	2005/05/18 13:15
L2	1177	"embedded processor"	USPAT	OR	OFF	2005/05/18 13:15
L3	249	"on-chip processor"	USPAT	OR	OFF	2005/05/18 13:15
L4	1423	l2 or l3	USPAT	OR	OFF	2005/05/18 13:15
L5	0	l4 and l1	USPAT	OR	OFF	2005/05/18 13:16
L6	24660	"714".clas.	USPAT	OR	OFF	2005/05/18 13:16
L7	152	l6 and l4	USPAT	OR	OFF	2005/05/18 13:18
L8	7	l7 and (pseudo-random)	USPAT	OR	OFF	2005/05/18 13:19